CLAIMS

What is claimed is:

1. A memory circuit, comprising:

a first electrode formed on a support surface, the first electrode having a first electrode surface that intersects the support surface;

a spacer positioned on the support surface adjacent to the first electrode surface; and

a ferroelectric layer formed on the first electrode and the spacer.

2. The memory circuit of claim 1, further comprises a second electrode formed on the ferroelectric layer opposite of the first electrode.

3. The memory circuit of claim 1, wherein the spacer comprises of an insulation material.

4. The memory circuit of claim 1, wherein the ferroelectric layer comprises of a polymer.

5. The memory circuit of claim 1, wherein the support surface comprises of insulation material.

6. The memory circuit of claim 1, wherein a portion of the spacer nearest to the first electrode surface has a height about equal to a height of the first electrode, the height of the first electrode being a distance between the support surface and a second electrode surface of the first electrode, the second electrode surface being substantially parallel to the support surface.

7. The memory circuit of claim 1, wherein the spacer is in contact with the first electrode surface.

8. The memory circuit of claim 1, wherein the spacer is separated from the first electrode surface.

9. The memory circuit of claim 1, wherein the support surface is located on a die.

10. The memory circuit of claim 1, wherein the spacer is formed for a selected one of moving a transition point away from the first electrode, and reducing sharpness of a transition.

11. The memory circuit of claim 1, wherein the first electrode comprises first and second portions, the first portion comprising a first material that is non-reactive to the ferroelectric layer and located at a second electrode surface of the first electrode, the second electrode surface being parallel to the support surface, and the second portion comprising a second material that is more conductive than said first material and located between the first portion and the support surface.

12. The memory circuit of claim 11, wherein the spacer is formed against the first electrode surface such that the spacer isolates the second portion from the ferroelectric layer.

13. A method, comprising:

forming a first electrode on a support surface, the first electrode having a first electrode surface that intersects the support surface;

forming a spacer positioned on the support surface adjacent to the first electrode surface; and

forming a ferroelectric layer on the first electrode and the spacer.

14. The method of claim 13, further comprises forming a second electrode on the ferroelectric layer opposite of the first electrode.

15. The method of claim 13, wherein said forming of a spacer comprises forming a portion of the spacer nearest to the first electrode surface with a height about equal to a height of the first electrode, the height of the first electrode being a distance between the support surface and a second electrode surface of the first electrode, and the second electrode surface being substantially parallel to the support surface.

16. The method of claim 13, wherein said forming of a spacer comprises forming the spacer by plasma enhanced chemical vapor deposition.

17. The method of claim 13, wherein said forming of a spacer comprises forming the spacer by depositing a spacer material on and around the first electrode and removing spacer material from a second electrode surface of the first electrode that is parallel to the support surface.

18. The method of claim 17, wherein the removing of the spacer material from the second electrode surface comprises removing the spacer material by a selected one of dry and wet etch.

19. The method of claim 13, wherein said forming of a spacer comprises forming the spacer for a selected one of moving a transition point away from the first electrode and reducing sharpness of a transition.

20. The method of claim 13, wherein said forming of a ferroelectric layer comprises forming the ferroelectric layer by spincoating.

21. A system, comprising:

an integrated circuit, including

a first electrode formed on a support surface, the first electrode having a first electrode surface that intersects the support surface,

a spacer positioned on the support surface adjacent to the first electrode surface, and

a ferroelectric layer formed on the first electrode and the spacer;

a bus coupled to the integrated circuit; and

a networking interface coupled to the bus.

22. The system of claim 21, wherein the integrated circuit further comprises a second electrode formed on the ferroelectric layer opposite of the first electrode.

23. The system of claim 21, wherein the spacer comprises an insulation material.

24. The system of claim 21, wherein the ferroelectric layer comprises a polymer.

25. The system of claim 21, wherein the support surface comprises an insulation material.